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FORM PTO-1390 (REV 10-95) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371

ATTORNEY DOCKET NUMBER: 96790P372

U.S APPLICATION NO. (If known, see 37 CFR 1.5): 09/913779

INTERNATIONAL APPLICATION NO.	INTERNATIONAL FILING DATE	PRIORITY DATE CLAIMED
PCT/JP99/00643	February 15, 1999	

TITLE OF INVENTION: SEMICONDUCTOR PRESSURE SENSOR - UTILITY

APPLICANT(S) FOR DO/EO/US: Masayuki Yoneda; Nobuaki Honda; Takeshi Fukiura; Shoji Nagasaki

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. ☒ This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.
2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.
3. ☐ This express request to begin national examination procedures (35 U.S.C. 371(f)) at any time rather than delay examination until the expiration of the applicable time limit set in 35 U.S.C. 371(b)) and PCT articles 22 and 39(1).
4. ☒ A proper Demand for International Preliminary Examination was made by the 19th month from the earliest claimed priority date.
5. ☐ A copy of the International Application as filed (35 U.S.C. 371(c)(2)).
   a. ☐ is transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☐ has been transmitted by the International Bureau.
   c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US).
6. ☒ A translation of the International Application into English (35 U.S.C. 371(c)(2)).
7. ☐ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371(c)(3)).
   a. ☐ is transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☐ have been transmitted by the International Bureau.
   c. ☐ have not been made; however, the time limit for making such amendments has NOT expired.
   d. ☐ have not been made and will not be made.
8. ☐ A translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).
9. ☒ An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4)).
10. ☐ A translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371(c)(5)).

Items 11. to 16. below concern document(s) or information included:

11. ☒ An Information Disclosure Statement under 37 CFR 1.97 and 1.98.
12. ☐ An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.
13. ☐ A FIRST preliminary amendment.
    ☐ A SECOND or SUBSEQUENT preliminary amendment.
14. ☐ A subsequent specification.
15. ☐ A change of power of attorney and/or address letter.
16. ☒ Other items or information:

priority request; formal drawings transmittal; 5 drawings sheets; petition for PCT aplication; international search report; cover page of pct application; notification of transmittal of copies of translation of the international preliminary examination report

U.S. APPLICATION NO (if known, see 37 CFR 1.5)	INTERNATIONAL APPLICATION NO	ATTORNEY'S DOCKET NUMBER
09/913779	PCT/JP99/00643	96790P372

17. ☒ The following fees are submitted:

BASIC NATIONAL FEE (37 CFR 1.492 (a) (1) - (5)):

		CALCULATIONS FOR PTO USE ONLY
Neither international preliminary examination fee (37 CFR 1.482 nor international search fee (37 CFR 1.445(a)(2)) paid to USPTO and International Search Report not prepared by EPO or JPO	**$1000.00**	
International preliminary examination fee (37CFR1.482)not paid to USPTO but International Search Report prepared by the EPO or JPO....	**$860.00**	
International preliminary examination fee (37 CFR 1.482) not paid to USPTO but international search fee paid to USPTO (37 CFR 1.445(a)(2))	**$700.00**	
International preliminary examination fee paid to USPTO (37 CFR 1.482) but all claims did not satisfy provisions of PCT Article 33(1)-(4)	**$690.00**	
International preliminary examination fee paid to USPTO (37 CFR 1.482) and all claims satisfied provisions of PCT Article 33(1)-(4)	**$100.00**	

ENTER APPROPRIATE BASIC FEE AMOUNT =				$	860.00
Surcharge of **$130.00** for furnishing the oath or declaration later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492(e)).				$	
CLAIMS	NUMBER FILED		NUMBER EXTRA	RATE	
Total claims	7	- 20 =	0	X **$18.00**	$ 0.00
Independent claims	1	- 3 =	0	X **$78.00**	$ 0.00
MULTIPLE DEPENDENT CLAIM(S) (if applicable)				+ **$270.00**	$
TOTAL OF ABOVE CALCULATIONS =				$	860.00
Reduction of 1/2 for filing by small entity, if applicable. Verified Small Entity Statement must also by filed (Note 37 CFR 1.9, 1.27, 1.28).				$	
SUBTOTAL =				$	860.00
Processing fee of **$130.00** for furnishing the English translation later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492(f)). +				$	
TOTAL NATIONAL FEE =				$	860.00
Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31). **$40.00** per property +				$	
TOTAL FEES ENCLOSED =				$	860.00
				$ Amount to be: refunded	$
				charged	$

a. ☒ A check in the amount of $ 860.00 to cover the above fees is enclosed.

b. ☐ Please charge my Deposit Account No. _____ in the amount of $_____ to cover the above fees. A duplicate copy of this sheet is enclosed.

c. ☒ The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. 022666. A duplicate copy of this sheet is enclosed.

NOTE: Where an appropriate time limit under 37 CFR 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the application to pending status.

SEND ALL CORRESPONDENCE TO:

Blakely, Sokoloff, Taylor & Zafman LLP
12400 Wilshire Blvd. 7th Floor
Los Angeles, CA 90025-1026

SIGNATURE

Eric S. Hyman
NAME

30,139
REGISTRATION NUMBER

U.S. APPLICATION NO. (if known, see 37 CFR 1.5)	INTERNATIONAL APPLICATION NO	ATTORNEY S DOCKET NUMBER
09/831779	PCT/JP99/00643	96790P372

17. ☒ The following fees are submitted:

BASIC NATIONAL FEE (37 CFR 1.492 (a) (1) - (5)):

		CALCULATIONS FOR PTO USE ONLY
Neither international preliminary examination fee (37 CFR 1.482 nor international search fee (37 CFR 1.445(a)(2)) paid to USPTO and International Search Report not prepared by EPO or JPO	$1000.00	
International preliminary examination fee (37CFR1.482)not paid to USPTO but International Search Report prepared by the EPO or JPO....	$860.00	
International preliminary examination fee (37 CFR 1.482) not paid to USPTO but international search fee paid to USPTO (37 CFR 1.445(a)(2))	$700.00	
International preliminary examination fee paid to USPTO (37 CFR 1.482) but all claims did not satisfy provisions of PCT Article 33(1)-(4)	$690.00	
International preliminary examination fee paid to USPTO (37 CFR 1.482) and all claims satisfied provisions of PCT Article 33(1)-(4)	$100.00	

ENTER APPROPRIATE BASIC FEE AMOUNT =	$	860.00
Surcharge of **$130.00** for furnishing the oath or declaration later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492(e)).	$	

CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE		
Total claims	7 - 20 =	0	X $18.00	$	0.00
Independent claims	1 - 3 =	0	X $78.00	$	0.00
MULTIPLE DEPENDENT CLAIM(S) (if applicable)			+ $270.00	$	

TOTAL OF ABOVE CALCULATIONS =	$	860.00
Reduction of 1/2 for filing by small entity, if applicable. Verified Small Entity Statement must also by filed (Note 37 CFR 1.9, 1.27, 1.28).	$	
SUBTOTAL =	$	860.00
Processing fee of **$130.00** for furnishing the English translation later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492(f)). +	$	
TOTAL NATIONAL FEE =	$	860.00
Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31). **$40.00** per property +	$	
TOTAL FEES ENCLOSED =	$	860.00
	$ Amount to be: refunded	$
	charged	$

a. ☒ A check in the amount of $ 860.00 to cover the above fees is enclosed.

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Los Angeles, CA 90025-1026

SIGNATURE

Eric S. Hyman
NAME

30,139
REGISTRATION NUMBER

DESCRIPTION

Semiconductor pressure sensor

1. Technical Field

This invention relates to a semiconductor pressure sensor. More specifically, the present invention is directed to a semiconductor pressure sensor of the type which uses strain gauges formed on a silicon diaphragm.

2. Background Art

Conventionally, a semiconductor pressure sensor using strain gauges is known. The pressure sensor forms a pressure-sense diaphragm on a silicon substrate. And, sensor elements (piezo-resistive devices) comprised by diffusion resistor layer are provided on the pressure-sense diaphragm. The variation of a pressure is measured by the detection of the distortion in the diaphragm.

Fig. 7 is a perspective diagram showing a semiconductor pressure sensor using conventional strain gauges. A part of the pressure sensor is shown by the cross section. As shown in Fig. 7, a sensor chip 200 is made by a silicon base 101 which has a diaphragm 110, and sensor elements on the diaphragm 110. The diaphragm 110 provides the whole center section of the silicon base 101 with a thin film, excluding a circumference part. A Wheatstone Bridge circuit 113 is comprised by strain gauges

105a-105d made from diffusion resistors, a metal wiring 103, and terminals 104a-104d.

Fig. 8 is a circuit diagram showing the Wheatstone Bridge circuit 113 based on Fig. 7. As shown in the diagram, the strain gauges 105a-105d made from diffusion resistors are respectively connected by the metal wiring 103. Terminals 104a-104d are provided between each strain gauge. Terminal 104a is connected to a power supply (high potential side). Moreover, terminal 104c is connected to a ground (low potential side). Therefore, a variation of resistance in strain gauges 105a-105d is performed by the deformation of the diaphragm 110 of Fig. 7. The voltage value between terminals 104b and 104d varies. The variation of a pressure is measured by the detection of change in voltage.

In the meantime, the sensor chip 200 is fixed on a pedestal 111, such as Pyrex (TM) glass. And, the sensor chip 200 is sealed in a package together with a silicon sealing liquid. The pedestal 111 provides a through-hole 112 for extracting air. The sensor chip 200 is attached so that the through-hole 112 may be covered. The silicon sealing liquid (not illustrated) is maintained on the diaphragm 110. The sensor elements on the diaphragm 110 (each member which comprises the Wheatstone Bridge circuit 113) is isolated from an external field. Therefore, the variation of a pressure is transmitted to the sensor elements via the silicon sealing liquid.

3. Disclosure of Invention

[Problem to be solved]

The pressure sensor as shown above needs a fine pattern process of the silicon substrate for formation of the diaphragm and the diffusion resistors, and is made from the semiconductor manufacturing process which must be considered sufficiently dustproof. However, even though the present clean room provides means for preventing dust, a trace metal-impurity enters into wafer or is generated midway through a process . As a result, the metal-impurity may bring on a fluctuation in a sensor output.

In general, when various semiconductor devices, such as MOSFET or the like are manufactured, a removal in the influence of a device etc. is performed by capturing the metal-impurity during manufacturing process of the wafer. This is called gettering. From the difference of the principle, it is classified into EG (extrinsic gettering) method and IG (intrinsic gettering) method. EG method is the technique which roughens a wafer back-side using a sandblasting method etc. to collect the impurity in the roughened-surface. IG method is the technique which makes inside the wafer many micro defects by precipitates of oxygen to capture the impurity in the micro defects.

However, the semiconductor pressure sensor with the structure which provides the strain gauges on the diaphragm etches most silicon-substrate back-sides to form the diaphragm. For this reason, even though gettering is performed in the wafer using conventional EG method and IG method, a getter reduces at the time of a formation of the diaphragm. Therefore, it

becomes difficult to capture the impurity sufficiently. Moreover, a new process for making the getter is required. There is also a problem that an effect changes with varieties of the wafer (a bare substrate, SOI (Silicon On Insulator) substrate, epitaxial substrate, etc.).

[Means for solving the problem]

The invention is made in order to solve such a problem, and an object of the present invention is to provide a semiconductor pressure sensor in which fluctuation in a sensor output is difficult to be produced.

A semiconductor pressure sensor according to the present invention comprises a Silicon substrate (1) with a diaphragm (10) which produces a distortion depending on a pressure, strain gauges (5a, 5b, 5c, 5d) which are provided on the diaphragm (10) and are formed by diffusion resistors, a PN-junction area which is provided adjacent in the strain gauges (5a, 5b, 5c, 5d) and which the reverse bias is applied to.

The PN-junction area may comprise the boundary surface between the silicon base (1) and a diffusion layer (8) provided in the silicon base (1).

The diffusion layer (8) may be locally provided near the strain gauges (5a, 5b, 5c, 5d).

A plural pair of strain gauges (5a, 5b, 5c, 5d) may be provided.

The plural strain gauges (5a, 5b, 5c, 5d) may form Wheatstone Bridge circuits.

The PN-junction area may be provided only in the strain

gauge (5c) at the side of the large electrical potential difference with a substrate potential among the terminal (4a) at the side of a high electric potential in the Wheatstone Bridge circuit and the terminal at the side of a low potential (4c).

The diffusion layer (8) may be formed of the combination of the plural long and slender patterns which are an acute angle toward the strain gauges (5a, 5b, 5c, 5d).

4. Brief Description of Drawings

Fig. 1 is a top view showing a semiconductor pressure sensor according to Embodiment 1 of the present invention.

Fig. 2A is a sectional view taken in the line A-A' in FIG.1.

Fig. 2B is a sectional view taken in the line B-B' in Fig. 1.

Fig. 3 is a top view showing Embodiment 2 of the present invention.

Fig. 4 is a top view showing Embodiment 3 of the present invention.

Fig. 5 is a top view showing Embodiment 4 of the present invention.

Figs. 6A, 6B, and 6C are the top views showing Embodiment 5 of the present invention.

Fig. 7 is a perspective diagram showing a conventional semiconductor pressure sensor.

Fig. 8 is a circuit diagram showing a Wheatstone Bridge circuit formed on the diaphragm of Fig. 7.

5. Best Mode for Carrying Out the Invention

Hereafter, the preferred embodiments of the present invention will be explained in detail.

The inventors of the present application performed various experiments to develope a semiconductor pressure sensor which does not have a fluctuation in an output. As a result, the inventors discovered that the fluctuation of a sensor output was brought on by Fe(iron) atom among a number of metal-impurity . That is, it is found that Fe atom in a sensor chip is drawn to PN junctions such as a diffusion resistor resulting in producing a leak current or change in resistance value. If the metal-impurity represented by Fe atom exists in active Si(silicon), it will be the condition that it is easy to narrow a band gap to excite an electron. And furthermore, when movable ions, such as Na(natrium), are interposed under bias application at high temperature, movement of an electron is promoted and it results in the fluctuation.

Therefore, the fluctuation conditions of the sensor output are as follows. (1) Existence of metal-impurity, such as Fe atom. (2) Existence of movable ions, such as Na. (3) Temperature is 125℃ or more. (4) Application of a bias potential. The fluctuation produces when these four conditions are satisfied.

However, Fe atom is hardly included in usual CZ (Czochralski) wafer used. When a device is formed in a wafer, Fe atom is considered to enter in the wafer. In the manufacture apparatus, iron and SUS (stainless alloy) are used in all parts. even a pincette is made from SUS. Therefore, in all processes,

Fe atom is considered to adhere to the wafer and to diffuse inside the wafer at various heat process. Of course, although a precision cleaning in a furnace is performed before a heat process of the wafer in general, it is difficult to remove completely. This is similar also to Na atom. There is a possibility that it may enter from all places, such as the human being's skin surface and perspiration. A complete removal is difficult.

Therefore, the inventors developed a semiconductor pressure sensor with the getter for capturing a metal-impurity, considering the above facts.

[Embodiment 1]

Fig. 1 is a plan showing a semiconductor pressure sensor according to Embodiment 1 of the present invention. As shown in Fig. 1, a sensor chip 20 is made by n type silicon base 1. The whole center section except the circumference part of the silicon base 1 comprises a diaphragm 10 of a thin film. The diaphragm 10 is provided with strain gauges 5a-5d made by p type diffusion resistors, a lead portion 6 formed by the p+ type diffusion resistors, a metal wiring 3, and terminals 4a-4d made from a metal. In this way, a Wheatstone Bridge circuit is formed from the above-mentioned components. When the silicon base 1 is n type substrate, a diffusion resistor is formed by thermal diffusion or ion implantation of a boron or the like.

Fig. 2A is a sectional view along the A-A' line of Fig. 1. Fig. 2B is a sectional view along the B-B' line of Fig. 1. As

shown in Fig. 2A, the main surface of the silicon base 1 is provided with the strain gauge 5a made from p type diffusion layer, the lead portion 6 made from p+ type diffusion layer close to the strain gauge 5a, a getter 8 made from p+ type diffusion layer close to the lead portion 6.

And, the layer-insulation film 2 made from SiO_2 is provided on the main surface of the silicon base 1. The metal wiring 3, the terminal, etc. which comprise one part of such a Wheatstone Bridge circuit, are provided on the layer-insulation film 2. The lead portion 6 is electrically connected with the strain gauge 5a. Furthermore, the lead portion 6 is connected with the metal wiring 3 via the through-hole electrode 7 provided in the layer-insulation film 2. Moreover, as shown in Fig. 2B, the getter 8 is connected with the metal wiring 3 via the through-hole electrode 9 provided in the layer-insulation film 2. And, a reverse bias is applied to the getter 8 via terminal 4c.

Thus, in this embodiment, the getter 8, which has PN reverse bias potential, is provided in vicinity of the strain gauges 5a-5d. Therefore, the metal-impurities in the silicon base 1 (Fe atom, Na atom, etc.) are captured to a PN-junction area. In this way, the variation of the resistivity and the development of the leak current in the strain gauges 5a-5d are prevented.

[Embodiment 2]

Fig. 3 is a top view showing a semiconductor pressure sensor according to Embodiment 2 of the present invention. A getter

8 is made into the mesh-like layout as shown in the diagram. Therefore, since a contact area of the p+ type getter 8 and the n type silicon substrate 1 increases, namely, a PN-junction area is expanded, a gettering effect improves.

[Embodiment 3]

Fig. 4 is a top view showing a semiconductor pressure sensor according to Embodiment 3 of the present invention. As shown in the Fig. 4, A getter 8 is locally provided only on the periphery of the strain gauges 5a-5d. Although the getter 8 in Figs. 1 and 3 was provided over the main surface of the silicon substrate 1, a leak current increases with this formation. So that, there is a possibility that the power consumption of the entire chip may increase. Therefore, the getter 8 was locally provided on the periphery of the strain gauges 5a-5d such as in this embodiment. Of course, each getter is electrically connected with terminal 4c via the through-hole electrode 9. Therefore, PN reverse bias is applied to any getter.

In addition, in the Fig. 4, although each getter is connected by using an identical diffusion layer, instead of connecting by the diffusion layer, the metal wiring may be provided on the silicon substrate 1. Moreover, although the layout of the getter 8 is made into the shape of mesh, this invention includes the layout of the getter that is not made into the shape of mesh such as in Embodiment 1.

[Embodiment 4]

Fig. 5 is a top view showing a semiconductor pressure sensor according to Embodiment 4 of the present invention. As shown

in the Fig. 5, A getter 8 is provided only on the periphery of the strain gauges 5c and 5d near a ground side. Metal-impurity, such as iron is positive ions. Therefore, it can be easy to draw to a portion with a large reverse bias to a substrate potential, i.e., sensor element of the ground side. If the getter 8 more than required is provided as the above-mentioned, problems such as the increase of a leak current will be caused. Consequently, the increase of the power consumption of the entire chip can be prevented by providing the getter of necessary minimum in the ground side (low potential side).

In addition, although the layout of the getter 8 is made into the shape of mesh, this invention includes the layout of the getter which is not made into the shape of mesh such as in Embodiment 1.

[Embodiment 5]

Fig. 6A, 6B, and 6C are the top views showing a semiconductor pressure sensor according to Embodiment 5 of the present invention. In the Fig. 6A, 6B, and 6C, a getter has a plurality of the long and slender pattern which is an acute angle toward a strain gauge. It is found that Fe atom can be drawn to the edge of a diffusion resistor, i.e., PN-junction area. Consequently, it is effective if the layout of a getter 8 is performed so that PN-junction area can be taken larger to the strain gauge as shown in the Fig. 6A, 6B, and 6C.

As explained in the five embodiments, the present invention can capture the metal-impurity in a silicon substrate to prevent a leak current from generating by the work of the

PN-junction area provided in the diaphragm.

What is claimed is:

1. A semiconductor pressure sensor comprising:

a Silicon substrate (1) with a diaphragm (10) which produces a distortion depending on a pressure;

strain gauges (5a, 5b, 5c, 5d) which are provided on the diaphragm (10) and is formed by diffusion resistors;

a PN-junction area which is provided adjacent to the strain gauges (5a, 5b, 5c, 5d) and which the reverse bias is applied to.

2. A semiconductor pressure sensor claimed according to Claim 1, wherein

the PN-junction area comprises the boundary surface between the silicon substrate (1) and a diffusion layer (8) provided in the silicon substrate (1).

3. A semiconductor pressure sensor according to Claim 2, wherein

the diffusion layer (8) is locally provided near the strain gauges (5a, 5b, 5c, 5d).

4. A semiconductor pressure sensor according to Claim 1, wherein

a plurality of the strain gauges(5a, 5b, 5c, 5d)are provided.

5. A semiconductor pressure sensor according to Claim 4,

wherein

a plurality of the strain gauges(5a, 5b, 5c, 5d) form a Wheatstone Bridge circuit.

6. A semiconductor pressure sensor according to Claim 5, wherein

the PN-junction area is provided only in the strain gauge (5c) at the side of the large electrical potential difference with a substrate potential among a terminal (4a) at the side of a high electric potential in the Wheatstone Bridge circuit and the terminal at the side of a low potential (4c).

7. A semiconductor pressure sensor according to Claim 2, wherein

the diffusion layer (8) is formed of the combination of the multiple long and slender patterns which is an acute angle toward the strain gauges(5a, 5b, 5c, 5d).

Summary

A semiconductor pressure sensor comprises a Silicon substrate (1) with the diaphragm(10) which produces a distortion depending on a pressure , strain gauges (5a, 5b, 5c, 5d) which are provided on the diaphragm (10) and is formed by diffusion resistors, a PN-junction area which is provided adjacent in the strain gauges (5a, 5b, 5c, 5d) and which the reverse bias is applied to.

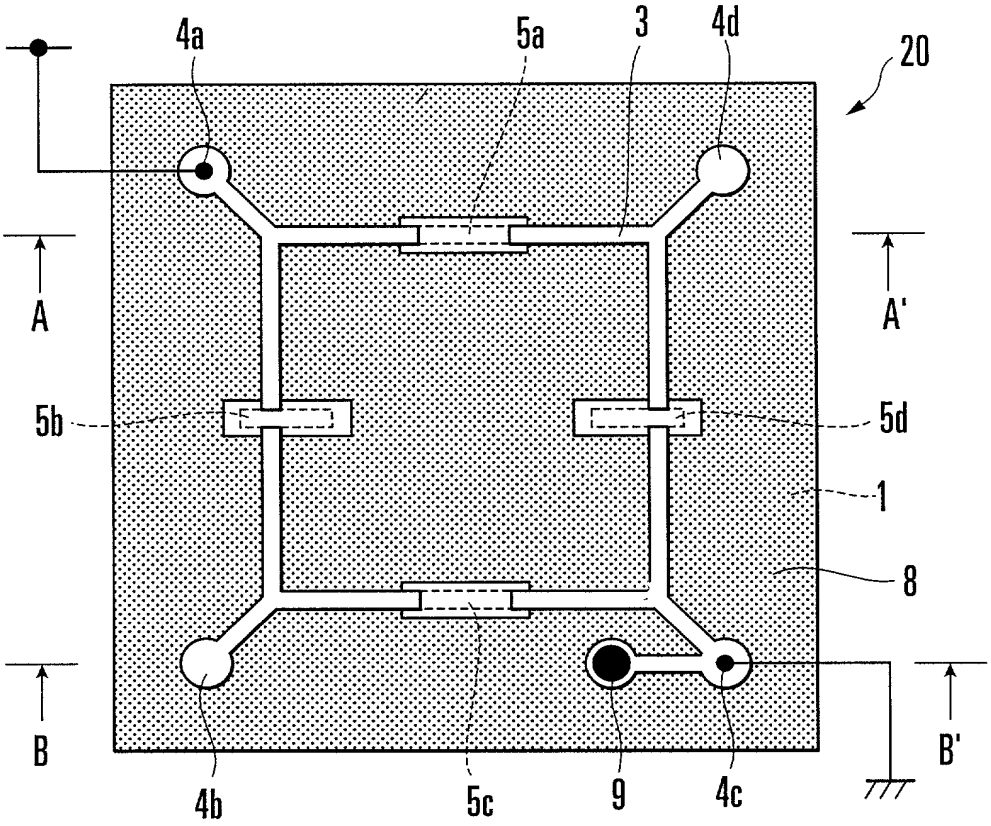

FIG. 1

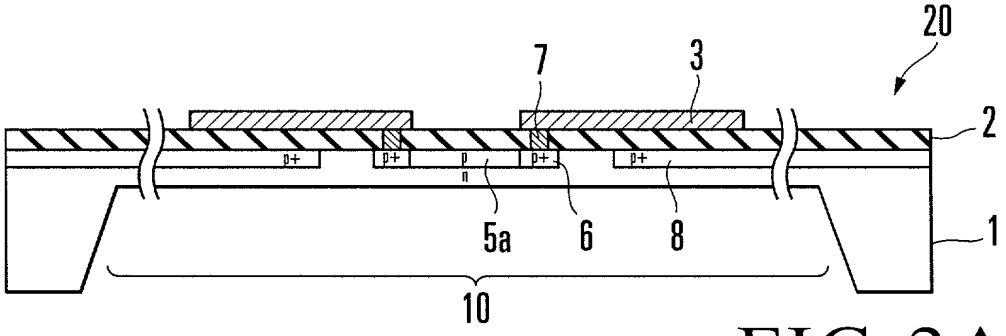

FIG.2A

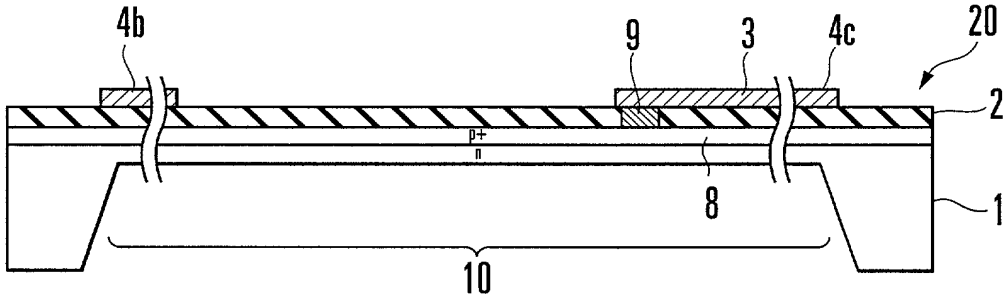

FIG.2B

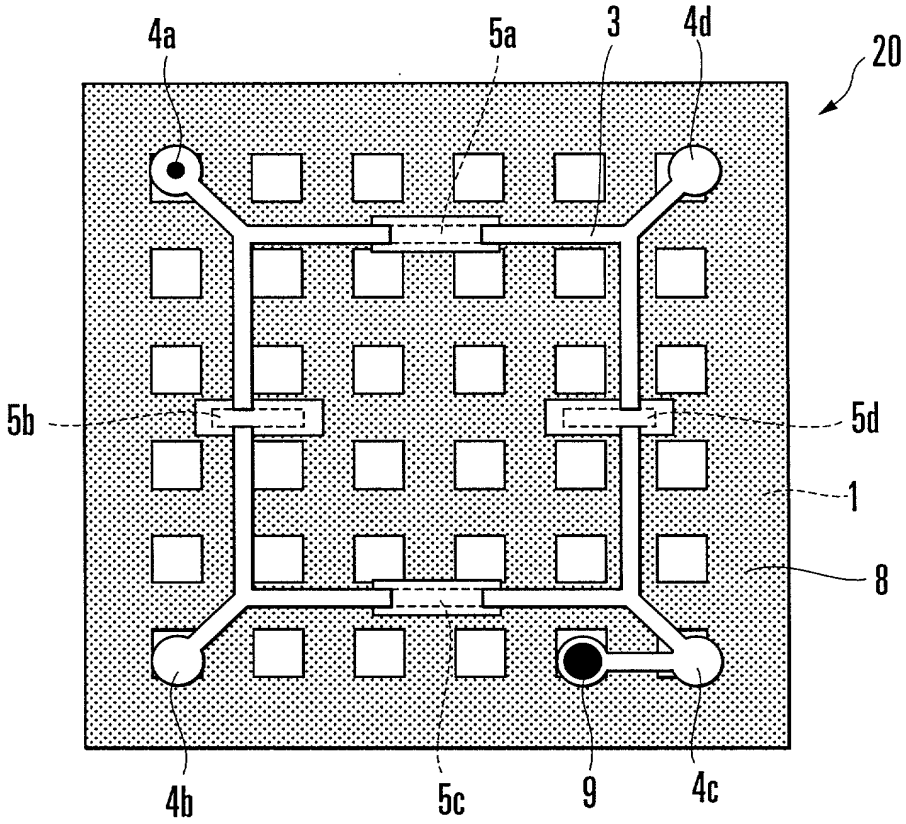

FIG. 3

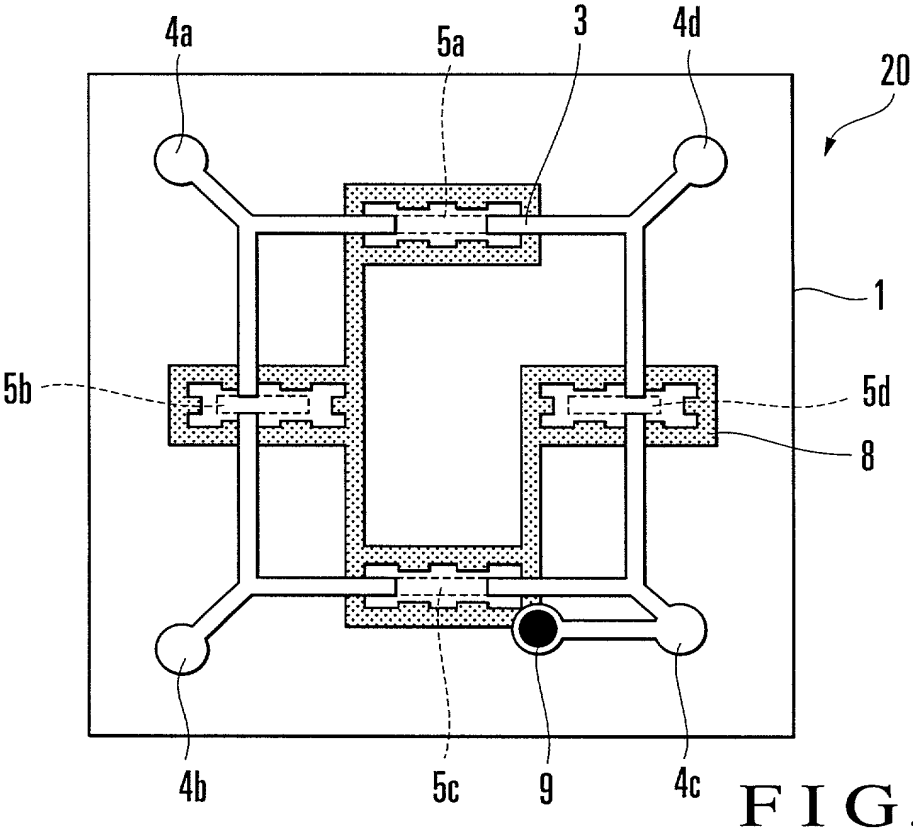

FIG. 4

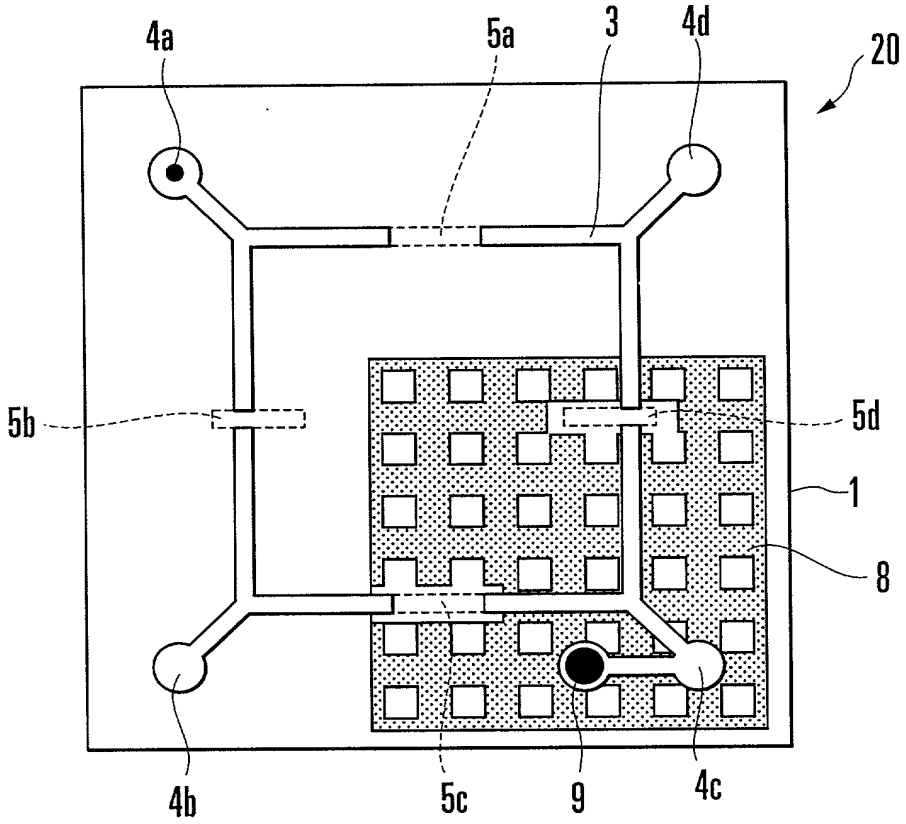

FIG. 5

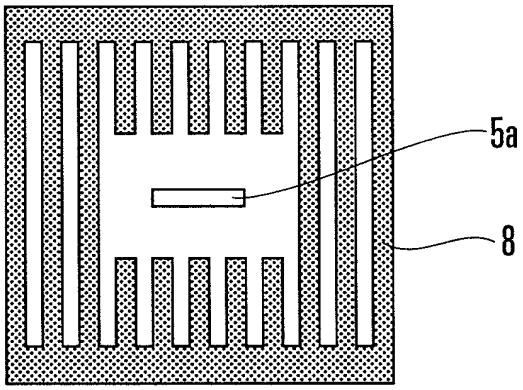

FIG.6(A)

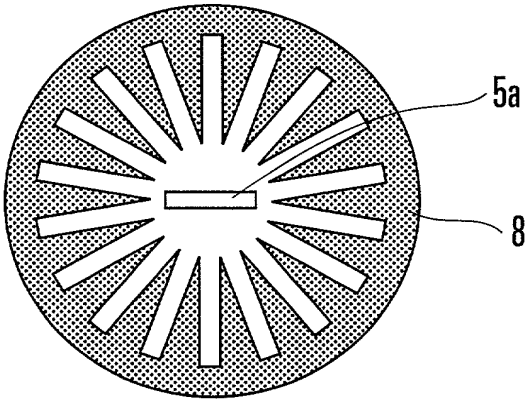

FIG.6(B)

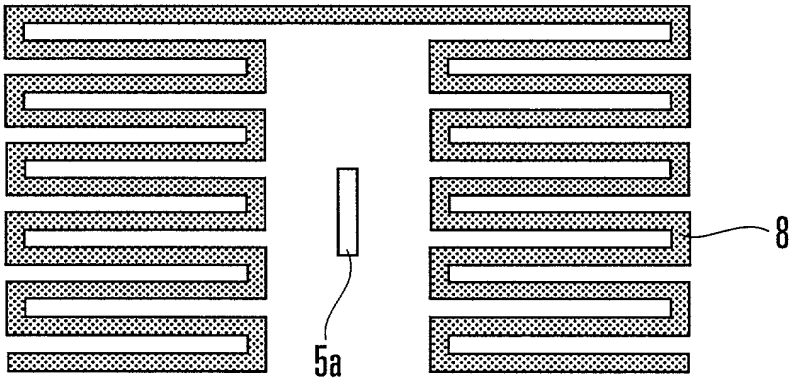

FIG.6(C)

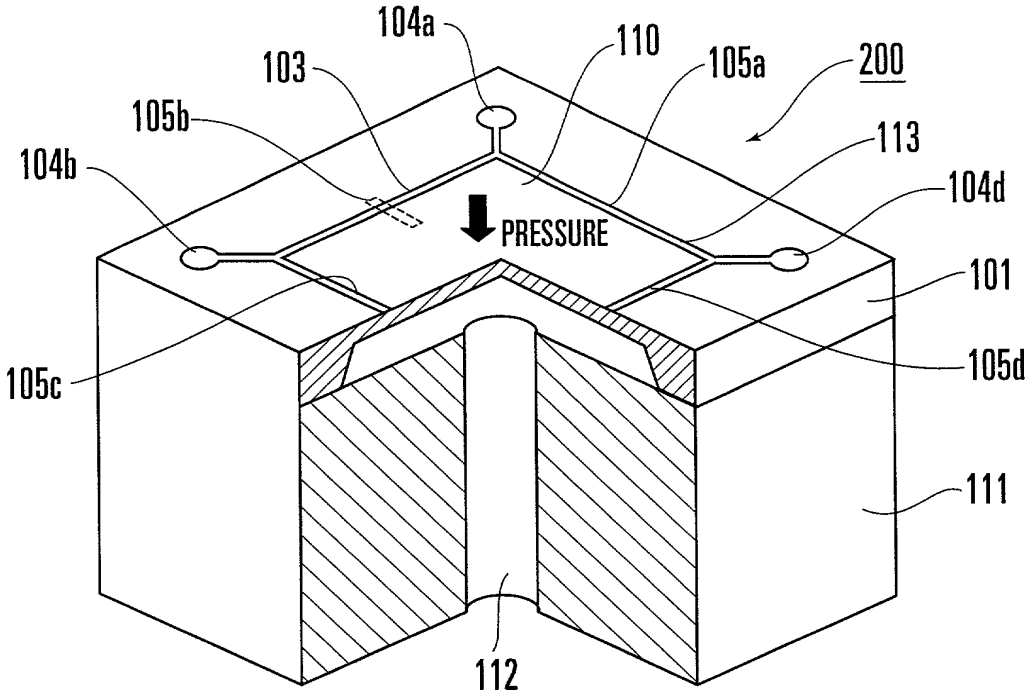
104a
110
103
105a
200
105b
113
104b
104d
PRESSURE
101
105c
105d
111
112

FIG. 7

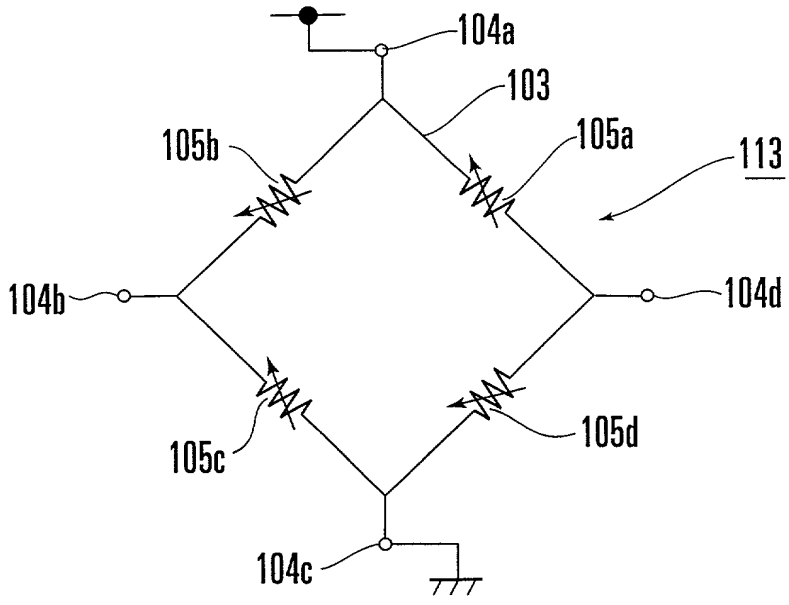
104a
103
105b
105a
113
104b
104d
105c
105d
104c

FIG. 8

#6

Attorney's Docket No.: 96790P372

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATI(

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below, next to my name.

I believe I am the original, first, and sole inventor (if only one name is listed below) or any original, first, an joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent i sought on the invention entitled

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the specification of which
☐ is attached hereto.
☒ was filed on **February 15, 1999** as
United States Application Number _____
or PCT International Application Number **PCT/JP99/00643**
and was amended on _____ .
(if applicable)

I hereby state that I have reviewed and understand the contents of the above-identified specification, includi the claim(s), as amended by any amendment referred to above. I do not know and do not believe that t claimed invention was ever known or used in the United States of America before my invention thereof, patented or described in any printed publication in any country before my invention thereof or more than o year prior to this application, that the same was not in public use or on sale in the United States of Ameri more than one year prior to this application, and that the invention has not been patented or made the subject an inventor's certificate issued before the date of this application in any country foreign to the United States America on an application filed by me or my legal representatives or assigns more than twelve months (fo utility patent application) or six months (for a design patent application) prior to this application.

I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Ti 37, Code of Federal Regulations, Section 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, Section 119(a)-(d), of any forei application(s) for patent or inventor's certificate listed below and have also identified below any forei application for patent or inventor's certificate having a filing date before that of the application on which prior is claimed:

Prior Foreign Application(s):

APPLICATION NUMBER	COUNTRY (OR INDICATE IF PCT)	DATE OF FILING (day, **month**, year)	PRIORITY CLAIMED
PCT/JP99/00643	WIPO	February 15, 1999	☐ No ☒ Yes
			☐ No ☐ Yes
			☐ No ☐ Yes

I hereby claim the benefit under Title 35, United States Code, Section 119(e) of any United States provisiona application(s) listed below:

APPLICATION NUMBER	FILING DATE

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States applicatio listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in prior United States application in the manner provided by the first paragraph of Title 35, United States Cc Section 112, I acknowledge the duty to disclose all information known to me to be material to patentabilit defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing dat the prior application and the national or PCT international filing date of this application:

P13363-A

(Application Serial No.)	(Filing Date)	(Status -- patented, pending, abandoned)
(Application Serial No.)	(Filing Date)	(Status -- patented, pending, abandoned)
(Application Serial No.)	(Filing Date)	(Status -- patented, pending, abandoned)

(40)

I hereby appoint BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN, a firm including: Aloysius T. C. AuYeung, Reg. No. 35,432; William Thomas Babbitt, Reg. No. 39,591; Jordan Michael Becker, Reg. No. 39,602; Bradley J. Bereznak, Reg. No. 33,474; ~~Michael~~ A. Bernadicou, Reg. No. 35,934; Roger W. Blakely, Jr., Reg. No. 25,831; Gregory D. Caldwell, Reg. No. 39,926; Kent M. Chen, Reg. No. 39,630; Lawrence M. Cho, Reg. No. 39,942; Thomas M. Coester, Reg. No. 39,637; Roland B. Cortes, Reg. No. 39,152; William Donald Davis, Reg. No. 38,428; Michael Anthony DeSanctis, Reg. No. 39,957; Daniel M. De Vos, Reg. No. 37,813; Tarek N. Fahmi, Reg. No. P41,402; James Y. Go, Reg. No. P40,621; David R. Halvorson, Reg. No. 33,395; Eric Ho, Reg. No. 39,711; George W Hoover II, Reg. No. 32,992; Eric S. Hyman, Reg. No. 30,139; Dag H. Johansen, Reg. No. 36,172; Stephen L. King, Reg. No. 19,180; Michael J. Mallie, Reg. No. 36,591; Kimberley G. Nobles, Reg. No. 38,255; Ronald W. Reagin, Reg. No. 20,340; James H. Salter, Reg. No. 35,668; William W. Schaal, Reg. No. 39,018; James C. Scheller, Reg. No. 31,195; Charles E. Shemwell, Reg. No. 40,171; Maria McCormack Sobrino, Reg. No. 31,639; Stanley W. Sokoloff, Reg. No. 25,128; Allan T. Sponseller, Reg. No. 38,318; Steven R. Sponseller, Reg. No. 39,384; Edwin H. Taylor, Reg. No. 25,129; Lester J. Vincent, Reg. No. 31,460; John Patrick Ward, Reg. No. 40,216; Ben J. Yorks, Reg. No. 33,609; and Norman ~~Zafman,~~ Reg. No. 26,250; my attorneys; and Robert Andrew Diehl, Reg. No. P40,992; Sharmini Nathan Green, Reg. No. P-41,410; Thomas A. Hassing, Reg. No. 36,159; Edwin A. Sloane, Reg. No. 34,728; and Judith A. Szepesi, Reg. No. 39,393; my patent agents, with offices located at 12400 Wilshire Boulevard, 7th Floor, Los Angeles, California 90025, telephone (310) 207-3800, with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected herewith.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

1-00

Full Name of First/Sole Inventor Masayuki Yoneda

Inventor's Signature Masayuki Yoneda Date October 29, 2001

Residence Kanagawa, Japan JPX Citizenship Japan

(City, State) (Country)

Post Office Address c/o FUJISAWAKOJO YAMATAKE CORPORATION, 1-12-2 Kawana, Fujisawa-shi Kanagawa 251-8522 Japan

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2-00

Full Name of Second/Joint Inventor Nobuaki Honda

Inventor's Signature Nobuaki Honda Date October 29, 2001

Residence Kanagawa, Japan JPX Citizenship Japan
(City, State) (Country)

Post Office Address c/o FUJISAWAKOJO YAMATAKE CORPORATION, 1-12-2 Kawana,
Fujisawa-shi Kanagawa 251-8522 Japan

3-00

Full Name of Third/Joint Inventor Takeshi Fukiura

Inventor's Signature Takeshi Fukiura Date October 29, 2001

Residence Kanagawa, Japan JPX Citizenship Japan
(City, State) (Country)

Post Office Address c/o FUJISAWAKOJO YAMATAKE CORPORATION, 1-12-2 Kawana,
Fujisawa-shi Kanagawa 251-8522 Japan

4-00

Full Name of Fourth/Joint Inventor Shoji Nagasaki

Inventor's Signature Shoji Nagasaki Date October 29, 2001

Residence Kanagawa, Japan JPX Citizenship Japan
(City, State) (Country)

Post Office Address c/o FUJISAWAKOJO YAMATAKE CORPORATION, 1-12-2 Kawana,
Fujisawa-shi Kanagawa 251-8522 Japan

Full Name of Fifth/Joint Inventor _____

Inventor's Signature _____ Date _____

Residence _____ Citizenship _____
(City, State) (Country)

Post Office Address _____

Full Name of Sixth/Joint Inventor _____

Inventor's Signature _____ Date _____

Residence _____ Citizenship _____
(City, State) (Country)

Post Office Address _____